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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Group Art Unit: 2816
Examiner: Linh M. Nguyen

In re PATENT APPLICATION of

Applicants:	Chen-Chih HUANG et al.	)
Serial No.:	10/773,450	)
Filed:	December 2, 2004	)
For:	PHASE-INTERPOLATION CIRCUIT	)
Atty Dkt:	SUND 501CIP	)

APPEAL BRIEF

October 15, 2007

Attn: Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTION

This is an Appeal to the Board of Patent Appeals and Interferences from the decision, in an Office Action dated April 13, 2007, finally rejecting claims 1-21 (all of the claims). A Notice of Appeal was filed on August 15, 2007, along with a Petition for two-month Extension of Time. Accordingly, it is respectfully submitted that the present Appeal Brief is timely.

A fee of $ 510 is being submitted concurrently. Should this remittance be accidentally missing, however, or should any additional fees be needed (including extension of time fees, since Appellants hereby provisionally petition for any extensions that may be deemed necessary to avoid abandonment), the Director may charge such fees to our Deposit Account number 18-0002.

(i) REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Realtek Semiconductor Corporation, having an office at No. 2, Industry E. Road, IX, Science-Based Industrial Park, Hsinchu 300, Taiwan, R.O.C.

(ii) RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of the undersigned attorney, there are no prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the pending appeal.

(iii) STATUS OF THE CLAIMS

Claims 1-21 are pending in this application. They have all been finally rejected. No claims have been cancelled, and no claims have been allowed. The final rejection of claims 1-21 is being appealed.

(iv) STATUS OF AMENDMENTS

A paper entitled "Response" was filed on June 13, 2007. It did not propose any revisions in the claims. An Advisory Action dated June 25, 2007 reported that the claims remained rejected.

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The present application is directed to a phase interpolation circuit. Such circuits can be used in a phase-interpolation signal generating device for producing signals with the same frequency but different phases.

The prior art arrangement shown in Figure 1A of the application's drawings has inverters 11 and 12 whose output terminals are connected together. The input terminals receive clock signals CK1 and CK2 with different phases. It will be apparent that when both CK1 and CK2 are high, the output Vo is low. Similarly, when CK1 and CK2 are both low, Vo is high. Because of the phase difference between CK1 and CK2, however, sometimes one clock signals is high while the other is low, and the output signal Vo reflects the resulting conflict between the inverters. The prior art arrangement, though, suffers from a periodic short-circuit current. This is shown schematically by an arrow in Figure 1B (page 6, lines 1-7).

Figure 3 of the application's drawings illustrates an embodiment of a phase interpolation circuit according to the present invention. This embodiment includes five inverters, 31-33, 36, and 37 (page 10, lines 13-15). Two of the inverters, 31 and 32, are connected between a first controlled switch 34 and a second controlled switch 35. Both of these controlled switches receive the output of inverter 36 as an input signal (page 11, lines 6-16).

The control switches 34 and 35 can be made from transistors, as shown in Figures 4A and 4B. By controlling the timing of switches 34 and 35 with the clock signal CK1, the short circuit current problem of the prior art can be avoided (page 12, lines 2-21).

The phase-interpolation signal generating device shown in Figure 8 of the application's drawings uses a plurality of phase interpolation circuits to generate eight multiphase signals CK0-CK7 based on four input multiphase signals CK0-CK3 (page 15, lines 12-15).

The independent claims are presented below, with annotations in parenthesis added to provide an example of how the claims can be read on the disclosure:

1. A phase-interpolation circuit (Figure 3) for outputting a third clock signal (331) according to a first clock signal (CK1) and a second clock signal (CK2), the circuit comprising:

a first inverter (31; page 10, lines 15-16) for receiving the first clock signal;

a second inverter (32; page 10, lines 16-17) for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end (30; page 10, line 17 to page 11, line 2) to output the third clock signal;

a first controlled switch (34; page 11, lines 6-10) coupled to the first inverter, the second inverter, and a power source (V_{DD}), wherein the first controlled switch is "off" when the first clock signal is in a first state, and is "on" when the first clock signal is in a second state; and

a second controlled switch (35; page 11, lines 10-14) coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch is "on" when the first clock signal is in the first state, and is "off" when the first clock signal is in the second state;

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal; and

wherein the first controlled switch and the second controlled switch serve to avoid a short-circuit current of the phase-interpolation circuit.

9. A phase-interpolation circuit (Figure 3) for outputting a third clock signal (331) according to a first clock signal (CK1) and a second clock signal (CK2), the circuit comprising:

a first inverter (31; page 10, lines 15-16) for receiving the first clock signal;

a second inverter (32; page 10, lines 16-17) for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end (30; page 10, line 17 to page 11, line 2) to output the third clock signal;

a first controlled switch (34; page 11, lines 6-10) coupled to the first inverter, the second inverter, and a power source (V_{DD}), wherein the first controlled switch is "off" when the first clock signal is in a first state, and is "on" when the first clock signal is in a second state; and

a second controlled switch (35; page 11, lines 10-14) coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch is "on" when the first clock signal is in the first state, and is "off" when the first clock signal is in the second state;

wherein the first controlled switch and the second controlled switch are to avoid a short-circuit current of the phase-interpolation circuit.

17. A phase-interpolation circuit (Figure 3) for outputting a third clock signal (331) according to a first clock (CK1) signal and a second clock signal (CK2), the circuit comprising:

a first inverter (31; page 10, lines 15-16) for receiving the first clock signal;

a second inverter (34; page 10, lines 16-17) for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end (30; page 10, line 17 to page 11, line 2) to output the third clock signal;

a first controlled switch (34; page 11, lines 6-10) coupled to the first inverter, the second inverter, and a power source (V_{DD}); and

a second controlled switch (35; page 11, lines 10-14) coupled to the first inverter, the second inverter, and a ground;

wherein the first controlled switch is turned "off" and the second controlled switch is turned "on" when the first clock signal is in a first state, and the first controlled switch is turned "on" and the second controlled switch is turned "off" when the first clock signal is in a second state.

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection: Claims 1, 4-9, 12-17 and 20-21 stand rejected under 35 USC 103 based on Applicants' admitted prior art (Figure 1A) in view of patent 6,198,334 to Tomobe et al. This prior art will hereafter be called simply "AAPA" and "Tomobe" for the sake of convenient discussion.

Second Ground of Rejection: Claims 2, 3, 10, 11, 18, and 19 stand rejected under 35 USC 103 based on the AAPA, Tomobe, and patent 6,225,847 to Kim. It is noted that this second ground of rejection will be contested in this Brief solely on the ground that the rejected claims are dependent claims.

(vii) ARGUMENT

The First Ground Of Rejection:

The AAPA has already been discussed, in section (v) of the Brief. The Tomobe reference is directed to a CMOS circuit with improved noise resistance. The embodiment shown in Figure 1 of the reference is an inverter with an additional PMOS transistor and an additional NMOS transistor. The two PMOS transistors in Tomobe's Figure 1 have

different switching speeds, as do the two NMOS transistors (see column 4, lines 24-29). The reference reports that the difference in switching speed "makes it difficult for the CMOS circuit to respond to a noise, thus enabling elimination of the noise" (column 2, lines 60-62). An Example is shown in Figure 2 of the reference, where "noise 1" and "noise 2" in the input signal results in noise at the level of transistor pairs (shown at the middle of Figure 2) but disappears in the output signal (shown at the bottom of Figure 1) due to the different switching speeds of the transistor pairs.

It is respectfully submitted that Tomobe has been inappropriately combined with the AAPA in the rejection. There are two reasons for this. First, there is no reason to think that an ordinarily skilled person might be worried about the noise in the clock signals CK1 and CK2 that are supplied to the AAPA as input signals. Why would an ordinarily skilled person ever encounter a noisy clock signal in actual practice? Secondly, Tomobe's scheme intentionally slows down the operation of his inverter. This slow-down might be acceptable in some situations, but would probably be unacceptable to an ordinarily skilled person who wanted an improved phase-interpolation signal generating device for producing multi-phase signals. The application advises that a typical use for multi-phase signals is with phase-locked loops, to shorten the lock-time or provide a plurality of receiving channels (page 3, lines 6-11). The ordinarily skilled person would want speed, and would be deterred by the delay that is an inherent feature of Tomobe's technique.

Even if an ordinarily skilled person did combine the references (despite the above argument to the contrary), it is respectfully submitted that he would still not arrived at the invention defined by the independent claims. Independent claim 1 provides that a "first controlled switch" is coupled to a first inverter, a second inverter, and a power source, and that a "second controlled switch" is coupled to the first inverter, the second inverter, and

ground. Claim 1 also provides that "the first controlled switch is 'off' when the first clock signal is in a first state, and is 'on' when the first clock signal in the second state," and that "the second controlled switch is 'on' when the first clock signal is in the first state, and is 'off' when the first clock signal is in the second state." Thus, both of the "controlled switches" recited in claim 1 respond to the same clock signal and are coupled to both the first inverter and the second inverter.

If an ordinarily skilled person replaced the inverters 11 and 12 in the AAPA with inverters as shown in Tomobe's Figure 1, the additional pair transistors in each of these replacement inverters would not receive the same clock signal. Nor would the additional pair of transistors in each Tomobe-type inverter control the power supplied to both of the Tomobe-type inverters. It is therefore respectfully submitted that Tomobe would not have led an ordinarily skilled person to modify AAPA so as to achieve invention defined by claim 1. The "first control switch" and the "second control switch" of claim 1 would not be present.

For similar reasons, it is respectfully submitted that independent claims 9 and 17 are patentable over the references. Claim 9 contains "first controlled switch" and "second controlled switch" recitations that are the same as claim 1, and similar limitations are included in a "first controlled switch" recitation, a "second controlled switch" recitation, and a "wherein" clause in claim 17. The rejection of independent claims 9 and 17 should therefore be reversed, along with the rejection of claim 1.

The remaining claims that are included in the first ground of rejection are dependent claims that are automatically patentable along with their independent claims. Nevertheless, several of the dependent claims will now be briefly addressed.

Claim 4 provides that the first controlled switch of claim 1 comprises a first PMOS coupled between the first inverter and the power source and a second PMOS coupled between the second inverter and the power source, with both PMOSs being turned on and off by the first clock signal. With the modification proposed in the Office Action, the additional PMOS transistors P1 in two of Tomobe's inverters would be controlled by different clock signals. Similar comments apply to dependent claim 6, which is directed to the second controlled switch of claim 1.

Claims 12 and 13 are similar to claims 4 and 5 but depend from claim 9 rather then claim 1. Claims 20 and 21 are also similar but depend from claim 17. These claims should be allowed for the same reasons discussed above with respect to claim 4 and 5.

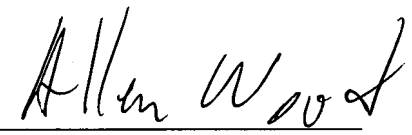
The Second Ground Of Rejection:

The claims included in the second ground of rejection are all dependent claims, so they are automatically patentable along with their independent claims. Since the independent claims are patentable for the reasons discussed above, the claims embraced by the second ground of rejection should also be allowed.

CONCLUSION

For the foregoing reasons, it is respectfully submitted that the Examiner's rejection of claims 1-21 for obviousness should be reversed.

Respectfully submitted,



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(viii) CLAIMS APPENDIX

The claims involved in this appeal are presented below.

1. A phase-interpolation circuit for outputting a third clock signal according to a first clock signal and a second clock signal, the circuit comprising:

a first inverter for receiving the first clock signal;

a second inverter for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal;

a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first controlled switch is "off" when the first clock signal is in a first state, and is "on" when the first clock signal is in a second state; and

a second controlled switch coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch is "on" when the first clock signal is in the first state, and is "off" when the first clock signal is in the second state;

wherein the phase of the third clock signal is determined by the phase of the first clock signal and the second clock signal; and

wherein the first controlled switch and the second controlled switch serve to avoid a short-circuit current of the phase-interpolation circuit.

2. The phase-interpolation circuit of claim 1, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

3. The phase-interpolation circuit of claim 1, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and

a fifth inverter to output the second clock signal to the second inverter.

4. The phase-interpolation circuit of claim 1, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state; and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state.

5. The phase-interpolation circuit of claim 1, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state; and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state.

6. The phase-interpolation circuit of claim 1, wherein the first controlled switch at least includes a PMOS.

7. The phase-interpolation circuit of claim 1, wherein the second controlled switch at least includes a NMOS.

8. The phase-interpolation circuit of claim 1, wherein the first and the second inverter are CMOS inverters.

9. A phase-interpolation circuit for outputting a third clock signal according to a first clock signal and a second clock signal, the circuit comprising:

a first inverter for receiving the first clock signal;

a second inverter for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal;

a first controlled switch coupled to the first inverter, the second inverter, and a power source, wherein the first controlled switch is "off" when the first clock signal is in a first state, and is "on" when the first clock signal is in a second state; and

a second controlled switch coupled to the first inverter, the second inverter, and ground, wherein the second controlled switch is "on" when the first clock signal is in the first state, and is "off" when the first clock signal is in the second state;

wherein the first controlled switch and the second controlled switch are to avoid a short-circuit current of the phase-interpolation circuit.

10. The phase-interpolation circuit of claim 9, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

11. The phase-interpolation circuit of claim 9, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and

a fifth inverter to output the second clock signal to the second inverter.

12. The phase-interpolation circuit of claim 9, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state; and

a second PMOS coupled between the second inverter and the power source, the second PMOS being "off" when the first clock signal is in the first state, and being "on" when the first clock signal is in the second state.

13. The phase-interpolation circuit of claim 9, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state; and

a second NMOS coupled between the second inverter and the ground, the second NMOS being "off" when the first clock signal is in the second state, and being "on" when the first clock signal is in the first state.

14. The phase-interpolation circuit of claim 9, wherein the first controlled switch at least includes a PMOS.

15. The phase-interpolation circuit of claim 9, wherein the second controlled switch at least includes a NMOS.

16. The phase-interpolation circuit of claim 9, wherein the first and the second inverter are CMOS inverters.

17. A phase-interpolation circuit for outputting a third clock signal according to a first clock signal and a second clock signal, the circuit comprising:

a first inverter for receiving the first clock signal;

a second inverter for receiving the second clock signal, wherein an output end of the second inverter is coupled to an output end of the first inverter to form a common output end to output the third clock signal;

a first controlled switch coupled to the first inverter, the second inverter, and a power source; and

a second controlled switch coupled to the first inverter, the second inverter, and a ground;

wherein the first controlled switch is turned "off" and the second controlled switch is turned "on" when the first clock signal is in a first state, and the first controlled switch is turned "on" and the second controlled switch is turned "off" when the first clock signal is in a second state.

18. The phase-interpolation circuit of claim 17, wherein the circuit further comprises a third inverter coupled to the common output end to output the third clock signal.

19. The phase-interpolation circuit of claim 17, wherein the circuit further comprises:

a fourth inverter to output the first clock signal to the first inverter; and

a fifth inverter to output the second clock signal to the second inverter.

20. The phase-interpolation circuit of claim 17, wherein the first controlled switch comprises:

a first PMOS coupled between the first inverter and the power source, the first PMOS being turned "off" when the first clock signal is in the first state, and being turned "on" when the first clock signal is in the second state; and

a second PMOS coupled between the second inverter and the power source, the second PMOS being turned "off" when the first clock signal is in the first state, and being turned "on" when the first clock signal is in the second state.

21. The phase-interpolation circuit of claim 17, wherein the second controlled switch comprises:

a first NMOS coupled between the first inverter and the ground, the first NMOS being turned "on" when the first clock signal is in the first state, and being turned "off" when the first clock signal is in the second state; and

a second NMOS coupled between the second inverter and the ground, the second NMOS being turned "on" when the first clock signal is in the first state, and being turned "off" when the first clock signal is in the second state.

(ix) EVIDENCE APPENDIX

No new evidence is being submitted with this Brief.

(x) RELATED PROCEEDINGS APPENDIX

In view of section (ii) of this Brief, no copies of decisions are appended.